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# Shaping Switching Waveforms in a 650 V GaN FET Bridge-Leg Using 6.7 GHz Active Gate Drivers

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**Abstract** — The application of active gate driving to 40 V GaN FETs has previously been shown to reduce ringing and EMI-generating spectral content in the switch-node voltage waveforms. This paper, for the first time, shows active gate driving applied to 650 V GaN FETs, and the shaping of device voltages and currents during switching transients. A custom integrated active gate driver is used, which can dynamically vary its output resistance from 0.12 to 64  $\Omega$ , with a 150 ps timing resolution.

At 200 V DC link and 10 A load current, a significant degree of control over the active-switch drain current and switch-node voltage is demonstrated, for both buck and boost mode operation. The current overshoot and ringing in the power waveforms due to circuit parasitics are actively reduced and the voltage oscillations in the DC link are damped. The timing of resistance sequences is shown to be critical to the success of active shaping methods, thus justifying the unparalleled 150 ps resolution of the driver.

Under continuous operation and at reduced ratings of 100 V and 2 A load current the significant control of the switch node voltage and voltage spectra is also demonstrated. The switching delay is reduced, and parts of the spectrum are reduced by up to 9 dB, equivalent to the effect of tripling the gate resistance but without any reduction in the overall switching speed.

**Keywords**—GaN; HFET; Wide Band-gap; Active Gate Driver; Gate Voltage Profiling; Drain Current Profiling; Switch Node Voltage Profiling; Oscillation Reduction; Arbitrary Gate Impedance; Dynamic Output Resistance; Programmable Gate Resistance

## I. INTRODUCTION

Active gate drivers shape a power device's switching waveforms during the switching transient, which is typically achieved by continuously varying gate resistance [1]–[7], gate voltage [8]–[10], or gate current [11]–[17]. This is in contrast to conventional gate drivers that apply a fixed voltage step function via a fixed resistance. With the move to faster switching wide-bandgap power devices, the need for waveform

shaping to help combat overshoots and ringing also increases. Active drivers for wide bandgap devices are emerging: those reported in [1],[18] change their output resistance at a single specific single point in the transient, for example in order to allow fast switching whilst avoiding gate voltage overshoot. Resistance sequences with multiple changeovers have been demonstrated in [5], however the updating of the resistance occurs every 40 ns, which is too infrequent for the active shaping of sub-10 ns GaN FET switching transients. Previous work by the authors [7], has demonstrated the first active gate driver with a bandwidth that is high enough to shape GaN FET waveforms during sub-10-ns switching transients. In [7], the focus lies on shaping gate and drain-source voltage waveforms on 40 V GaN devices, for example to reduce ringing.

This work demonstrates the shaping of both current and voltage waveforms in a mains-voltage bridge leg, using 650 V GaN FETs. The controllability over the drain current transient is important, as this contributes to EMI generation. Observing the transient current in the bridge also facilitates the developing of active gate driving strategies, as, for example at turn-on, the gate voltage of the control device directly influences this current, which, in turn, is the direct cause of the rise in the

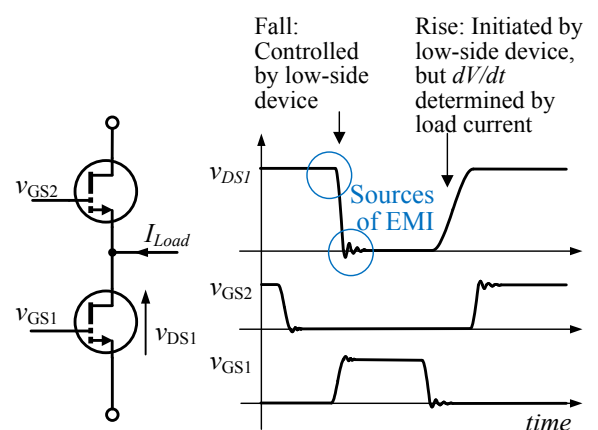


Fig. 1. Conceptual switch-node voltage transitions of a bridge-leg for current flowing into switch-node, with potential sources of EMI indicated, and the high- and low-side gate signals. Small  $v_{sw}$  changes, which occur when the high-side device's gate is turned on or off, are neglected for clarity.

drain-source voltage over the synchronous device. This transient is illustrated in Fig. 1.

Implementation in a hard-switched mains-voltage bridge-leg presents additional challenges, namely: the driver needs to work under level shifting with  $dv/dt$  approaching 100 V/ns; two gates are in control of the switch-node voltage; the control over each transient is only partial; and the devices' respective roles depend on the polarity of the load current, e.g.

Fig. 1 illustrates transients where the load current is flowing into the switch node (boost mode). Here, the low-side gate controls the falling edge of the switch-node transient, and its rising edge is slower and determined by the load current charging the output capacitances [19]. The situation for current flowing out of the switch-node is reversed.

Section II describes the custom active gate driver, Section III provides an overview of the experimental facility, and Section IV shows the experimental waveform shaping.

## II. HIGH-SPEED ACTIVE GATE DRIVER

Fig. 2 illustrates the programmable gate driver used in this work. Fabricated in AMS HVC MOS 180 nm technology, it integrates high-speed memory, a 400 MHz to 700 MHz voltage-controlled oscillator (VCO), hybrid synchronous and asynchronous control logic, and a dynamically-adjustable 120 m $\Omega$  to 64  $\Omega$  output stage, in a QFN32 surface-mounted package.

The output stage is connected directly to the gate of the power device and consists of two parallel-connected drivers: a “main” driver that operates synchronously, with  $2^8$  resistance levels; and a “fine” driver that operates asynchronously, with  $2^6$  resistance levels. Once the memory is programmed, the gate driver operates autonomously. On each PWM edge, a gate-drive sequence of 8 internal clock cycles duration (11.4 ns to 20 ns) is read from memory by the control logic, and appropriate control signals are applied to the output stages. The setting in the 8th clock period is maintained until the next PWM transition, and there are independent resistance sequences for low-high and high-low transitions.

For the “main” driver, the sequence defines one pull-up (for PWM low-high transition) or pull-down (for PWM high-low transition) resistance value per clock cycle. During each clock

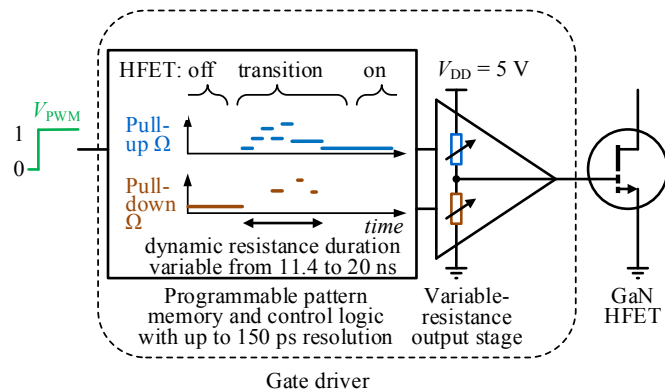


Fig. 2. Active gate driving principle used to control GaN FETs in this work.

cycle, further adjustments of the driver's output resistance can be made using the “fine” driver, with a timing resolution of 150 ps. This sub-clock resolution is achieved by means of asynchronous control circuits timed by digitally-selectable delay elements. The fine driver can pull up or down regardless of the state of the PWM, so can pull in the opposite direction to the main driver, if required. The output of the programmable driver can be set to a constant gate-drive strength to compare the results of active gate driving to conventional gate driving.

For this work the internal clocks of the gate drivers are set to ~620 MHz giving ~1.6 ns per main-driver resistance change and ~12.8 ns of control time during a GaN FET switching transition. This was chosen to provide the highest possible update resolution while the power device's gate-source signal is transitioning through the threshold voltage and the Miller plateau.

## III. TEST SETUP AND EXPERIMENTAL PROCEDURE

### A. Test Circuit

A clamped inductive switching circuit is employed to test active gate driving in high voltage GaN-based converters. Fig. 3 shows a schematic of the experimental circuit, with the possible configurations of the load inductors and resistors used for this work. The circuit is designed to be operated in both double-pulsed and continuous switching modes, with a choice of loads. For this work, double-pulse tests use purely inductive loads, and continuous switching uses an R-L-C composite load. This circuit is capable of replicating the device interactions and hard-switching transitions in a synchronous boost converter (load current flows into the switch node) or buck converter (load current flows out of the switch node), depending on the configuration of the load.

For boost mode, the lower device in the bridge leg ( $Q_1$ ) is the active switch and has its turn-on transition shaped by its gate driver. In this mode the active switch turn-off transition and both transitions of the synchronous switch ( $Q_2$ ) are driven with a fixed drive strength. A load inductor alone is connected

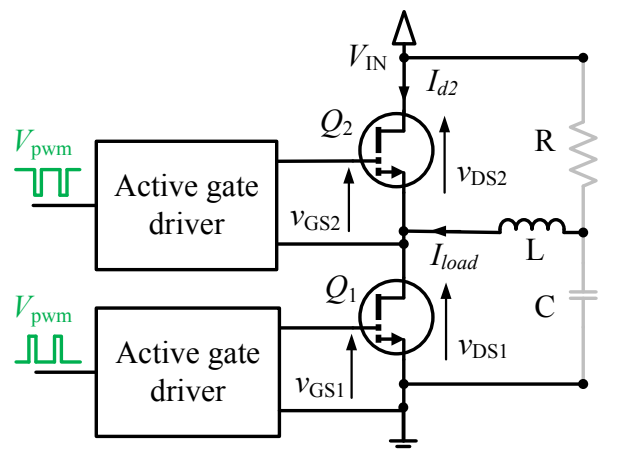


Fig. 3. Bridge leg arrangement and possible configurations of load components to cater for buck (current out of the switch node) or boost (current in to the switch node) mode and also continuous or double-pulsed operation.

between the positive DC Link and the switch node so that the load current is always flowing into the switch node.

For the double-pulsed Buck mode of operation,  $Q_2$  is now the active switch with its turn-on transition being shaped. As with the Boost mode configuration all other transitions occur with a fixed drive strength. The load inductor is now connected between the switch node and the negative DC Link to ensure current always flows out of the switch node. For continuous operation an L-C filter using a different inductor and a capacitor to the negative DC link is employed, with a load resistor connected to the positive DC Link resulting in current always flowing into the switch node.

Both high- and low-side active gate drivers, their support circuitry, and their power supplies are fully isolated so that all transitions in the bridge leg may be shaped and either side may be ground-referenced to allow flexibility in operation and measurement.

### B. Test Setup

The configuration of the experimental hardware is illustrated in Fig. 4. A Diligent Zedboard with a Xilinx Zync 7000 series system-on-chip (SoC) provides a user interface to configure the gate drivers and program them. Prior to testing, the host computer sends the desired drive sequences to the Xilinx system, which in turn programs the gate drivers. For a double-pulse experiment, an external Keysight 81150A function generator, which is configured with the desired double-pulse gate-driver control waveforms from MATLAB, has its output passed in to and through the Xilinx system to the gate drivers. For continuous switching tests, 100 kHz PWM signals are generated in the FPGA fabric of the Zync SoC.

Waveforms are captured and de-skewed on a Rhode & Schwarz RTO 1024 2 GHz 10 GSa/s oscilloscope. With the

low-side as the active switch, data capture triggering occurs on the second rising edge of  $v_{GS1}$ . For the high-side as the active switch, the rising edge of  $v_{DS1}$  is used as neither  $v_{DS2}$  nor  $v_{GS2}$  can be inspected directly. Wideband floating high-voltage measurements and non-invasive high-bandwidth current measurements are problematic and therefore single ended, ground-referenced voltage measurements are the primary data in this work. Voltages  $v_{DS1}$  and  $v_{GS1}$ , the low-side device drain-source and gate-source voltages, are measured with R&S RT-ZP10 10:1 500 MHz and PMK HV1000 100:1 400 MHz passive voltage probes respectively. Current information for  $i_{D2}$  is captured with a floating current probe developed in conjunction with RAM Innovation Ltd, with an insertion impedance of 0.2 nH at 1 GHz, and a bandwidth of 300 MHz.  $i_{D1}$  measurements are not taken directly. As the parasitic capacitance of the output inductor is very small, the output current is assumed to be constant during the switching transition, and thereby the drain current of the low-side control device is obtained by subtracting the measured high-side device current from the constant output current.

For continuous switching experiments, the oscilloscope is set to capture and average 8,192 consecutive waveforms in order to enhance the signal:noise ratio. Data are transferred to the host PC for conversion into the frequency domain using MATLAB.

The main power board is shown in Fig. 5. It contains two custom drivers, and two GaN Systems GS66508P 650 V 55 mΩ FETs.

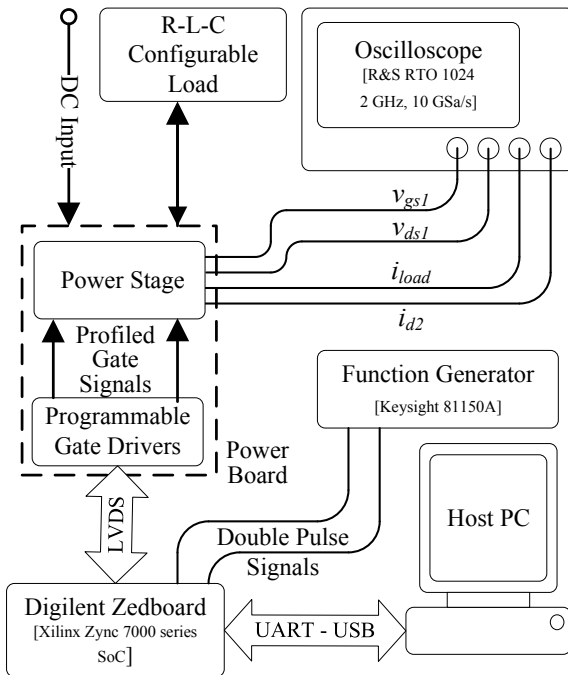


Fig. 4. Overview of the test system hardware layout and interconnects.

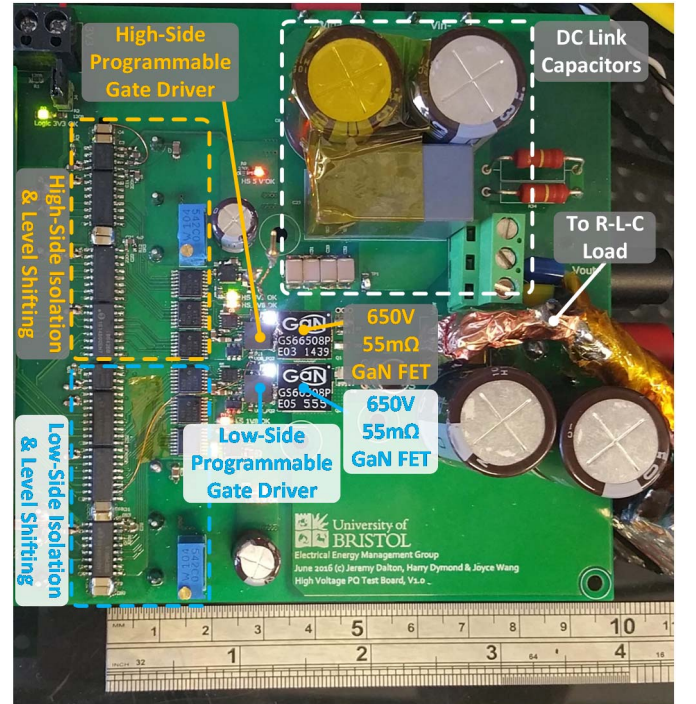


Fig. 5. Power board, containing bridge-leg consisting of two GaN Systems GS66508P 650 V 55 mΩ HFETs, each with its own programmable gate driver, isolated power supply, level shifting and isolation for control signals.



### C. Transitions Under Investigation and Shaping Strategy

In a bridge leg, there are four types of gate transitions per load current direction, as illustrated in Fig. 6, where dead times have been exaggerated for clarity. With the current flow representing boost conversion (Fig. 6 left), the low-side device is the control device. Its turn-on controls the switching transient, however at turn-off, the load current sets its device voltage gradient  $dv_{DS}/dt$ . Therefore the turn-on transient (highlighted) is more controllable and used in Section IV.A to demonstrate active gate driving. During buck conversion, with the load current flowing out of the switch node (Fig. 6 right), the high-side device is the control device. Turn-on (highlighted) is more controllable, and is therefore demonstrated in Section IV.B.

The shaping strategy employed is similar to the strategy for low voltage GaN devices reported in [7]. It can be summarized by the strong driving of the device up to its threshold voltage, a slow and precisely controlled transition through the miller plateau as  $v_{DS}$  falls, and then a final strong driving phase to raise  $v_{GS}$  to the maximum value.

## IV. RESULTS

### A. Double-Pulsed Boost Operation

For current flowing in to the switch node, the circuit is configured with load component values as shown in Table I. The DC link voltage is 200 Volts and the initial pulse charges the inductor current to 10 Amperes.

Fig. 7 shows the measured turn-on switching waveforms of the control device for one active gate-driving and two constant-strength scenarios. The aim of the active gate driving sequence

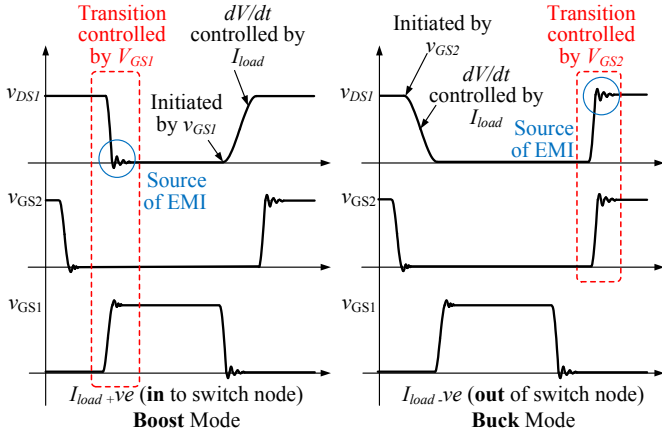


Fig. 6. The four switch-node voltage transitions that are possible in a bridge leg. Left: boost conversion with load current flowing into the switch node. Right: buck conversion with load current flowing out of the switch node.

TABLE I. CIRCUIT CONFIGURATION FOR DOUBLE-PULSED BOOST-MODE OPERATION

Component	Value
R	Short Circuit
L	88 $\mu$ H
C	Open Circuit

used here is to reduce current stress and current ringing in the bridge-leg. Driving the control GaN FET with a fixed strength of 7.2  $\Omega$  results in 18.9 A current ( $i_{D1}$ ) overshoot and ringing duration of more than 20 ns. Decreasing the drive strength to 18  $\Omega$  reduces the current overshoot to 10.2 A and damps the ringing by 73%, but increases the switching loss and switching time by 45% and 50% respectively.

The control-device's turn-on switching loss for each scenario has been estimated using [20]

$$E_{SWon} = \int (i_{D1} \times v_{DS1}) dt + E_{Coss}, \quad (1)$$

and is provided in the line labels of the  $v_{DS1}$  graph in Fig. 7.  $E_{Coss}$  is the energy that is stored in the output capacitance of the device in its off-state, and can be derived through simulation or using the datasheet [21]. For 200 V switching of GS66508P GaN devices,  $E_{Coss}$  is 2.9  $\mu$ J.

It is apparent that the active resistance sequence of Fig. 7 provides a reduction in current overshoot and ringing, without a significant increase in switching loss: A low resistance is applied for the first 1.6 ns of the switching transition to reduce the turn-on delay time and the initial current rise time. A subsequent increase of the resistance suppresses  $i_{D1}$  overshoot and in-circuit ringing and maintains the current slew rate the same as 7.2  $\Omega$  gate drive strength. Momentary decreases in the resistance are used to optimize the switching waveforms and reduce the overlap loss. The final decrease of drive resistance provides a strong pull-up for the remaining on-state. This strategy is seen to almost eliminate the ringing in the drain current and reduce its overshoot by 10%, however with no

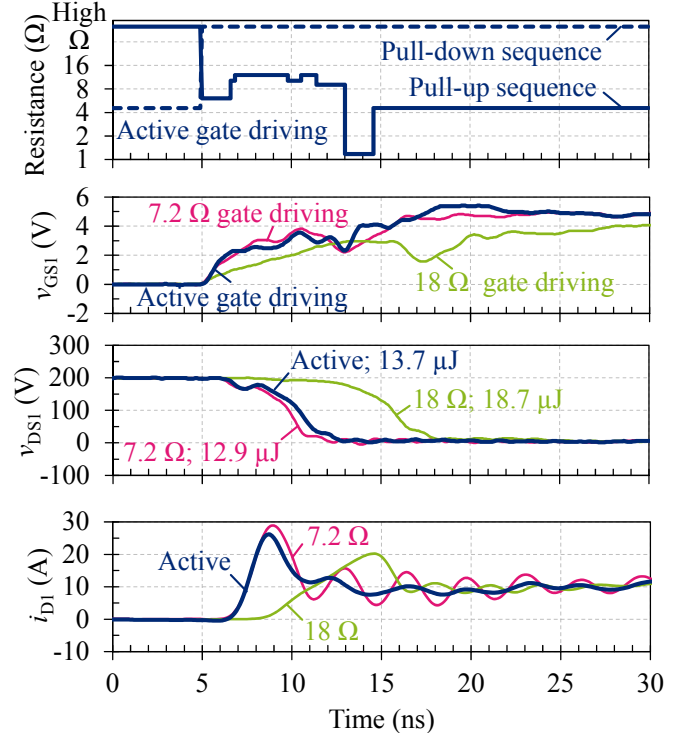


Fig. 7. Measured turn-on switching waveforms of the control device under boost-mode operation, with constant-strength gate driving (7.2  $\Omega$  and 18  $\Omega$ ), and active gate driving (gate resistance sequence plots at top) to reduce ringing in the drain current  $i_{D1}$  and switch-node voltage  $v_{DS1}$ .

increase in switching time and an increase in switching loss by only 6%. This is a significantly better trade-off of current ringing against switching loss than the  $18\ \Omega$  constant gate driving, which is one of the recommended values for the turn-on gate resistance for this particular power device [19].

Fig. 8 compares another active gate driving sequence to that of Fig. 7. The new sequence is seen to have the same damping effect on the drain current, but to further reduce the current overshoot to 12.4 A, and eliminate the overshoot in the gate-source voltage  $v_{GS1}$ . In exchange, the turn-on switching loss is increased by 7%. This illustrates a trade-off to be made when defining active gate driving sequences.

### B. Double-Pulsed Buck Operation

For current flowing out of the switch node, the circuit is configured with load component values as shown in Table II. The DC link voltage is 200 V and the initial pulse charges the inductor current to 10 A.

Fig. 9 shows an actively controlled transition compared against three transitions that use different constant driving strengths ( $9\ \Omega$ ,  $12\ \Omega$ , and  $18\ \Omega$ ). As in the previous set of

results, the current measurement represents the drain current of the control device as it takes up the load current out of the switch node, only that this is now the high-side device. The results show the following:

1. **Switching delay.** With an increasing in constant driver resistance, the drive strength decreases, and the time delays of  $i_{D2}$  and  $v_{DS1}$  increase. The delay with active gate driving is identical to that of the constant  $12\text{-}\Omega$  scenario, as the active driving sequence is initially set to  $12\ \Omega$ .
2. **Current overshoot.** Compared with the three constant gate driving scenarios, it is clear that that active driving sequence reduces the peak drain current  $i_{D2}$ .
3. **Ringing and EMI.** Active gate driving delivers a smoother  $i_{D2}$  waveform which is monotonic during the current rise with lower oscillation once it has fallen back to the level of the load current. The damping appears to be equivalent to that of the  $18\text{-}\Omega$  scenario. This smoother waveform will contain lower-magnitude high-frequency components and therefore generate less EMI [10]. Active gate driving also reduces and softens the peak of  $i_{D2}$ .

In light of these aspects, it can be concluded the active gate driving technique can control the profile of drain current  $i_{D2}$ , and provide a better trade-off, relative to fixed-strength driving, between time delay, current overshoot, ringing and EMI.

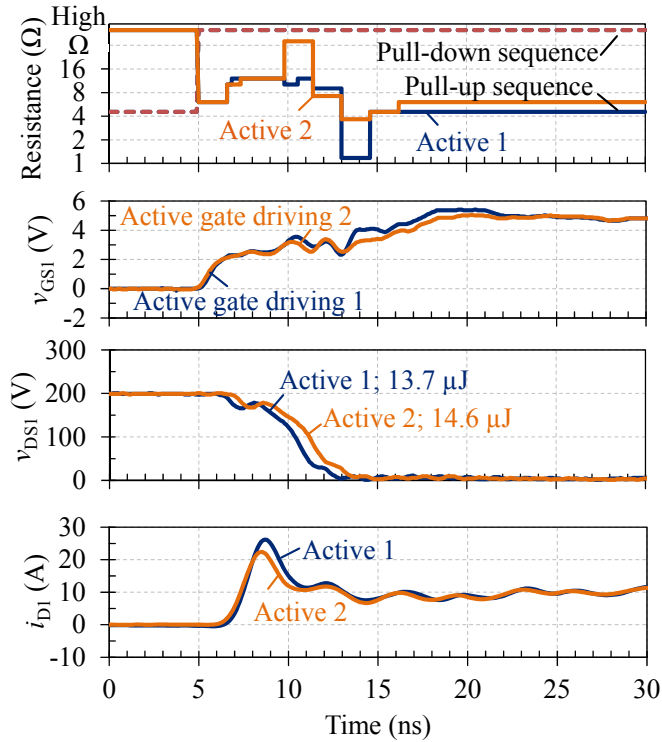


Fig. 8. Measured turn-on switching waveforms of the control device under boost conversion, with two active gate-driving scenarios (gate resistance sequence plots at top) to reduce ringing in the drain current  $i_{D1}$  and switch-node voltage  $v_{DS1}$ .

TABLE II. CIRCUIT CONFIGURATION FOR DOUBLE-PULSED BUCK-MODE OPERATION

Component	Value
R	Open Circuit
L	$88\ \mu\text{H}$
C	Short Circuit

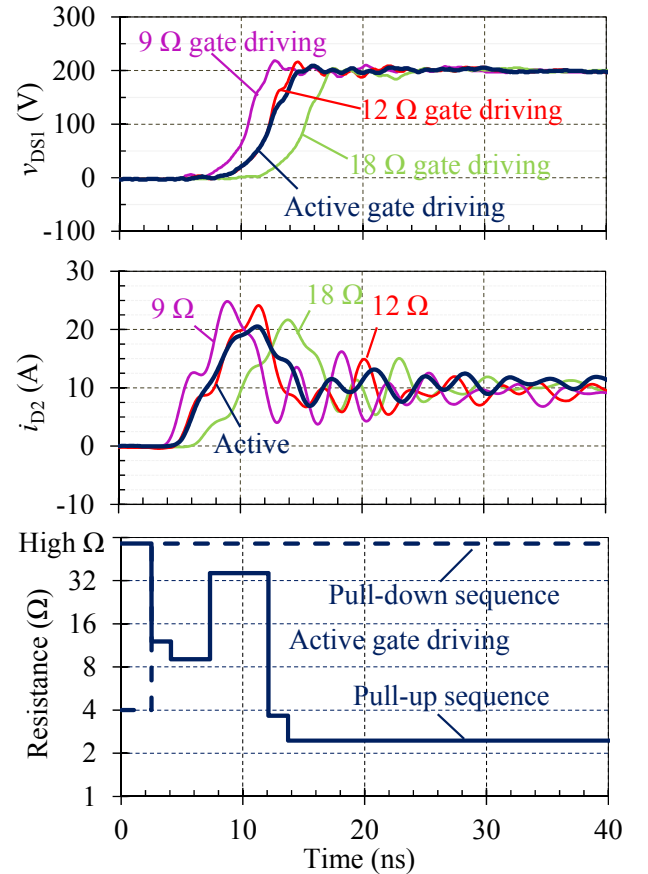


Fig. 9. Measured switching waveforms for the active switch current and synchronous switch voltage during active switch turn on under buck conversion. The gate-drive resistance sequence used for the active switch under the active gate-driving scenario is shown in the bottom plot.

### C. Continuous Boost Operation

For continuous boost operation, the circuit is configured with load component values as shown in Table III. The DC link voltage is 100 V and the duty cycle of the 100 kHz PWM control signal is set to give a DC load current of 2 A.

In this experiment, the aim is to turn on the control device as fast as when driven with a fixed 12  $\Omega$  resistance, however to obtain EMI-generating spectral components that are typical of slower 36  $\Omega$  driving. Fig. 10 shows the measured switch-node voltage  $v_{DS1}$  and the low-side gate voltage  $v_{GS1}$  under three different gate-drive scenarios: faster 12  $\Omega$  fixed driving, slower 36  $\Omega$  fixed driving, and active gate driving (thicker lines). The active driving scenario results in a 90 % to 10 % switch-node transition time of 5.6 ns, similar to the faster 12  $\Omega$  fixed drive. Delay is reduced by 3.3 ns with respect to the fast 36  $\Omega$  driving, due to the use of a lower initial gate-drive resistance to quickly ramp the device to its threshold voltage. Drive strength is then reduced during the transient in order to result in a less abrupt end to the switching transition.

Fig. 11 shows the influence the different gate-drive scenarios on the spectrum of the switch-node voltage. The spectral envelopes are calculated from the time-domain data of a complete switching cycle and therefore include contributions from the low-to-high transition. The nature of this edge is governed by the load current and is unaltered in all three

TABLE III. CIRCUIT CONFIGURATION FOR CONTINUOUS BOOST-MODE OPERATION

Component	Value
R	5 $\Omega$
L	44 $\mu$ H
C	66 $\mu$ F

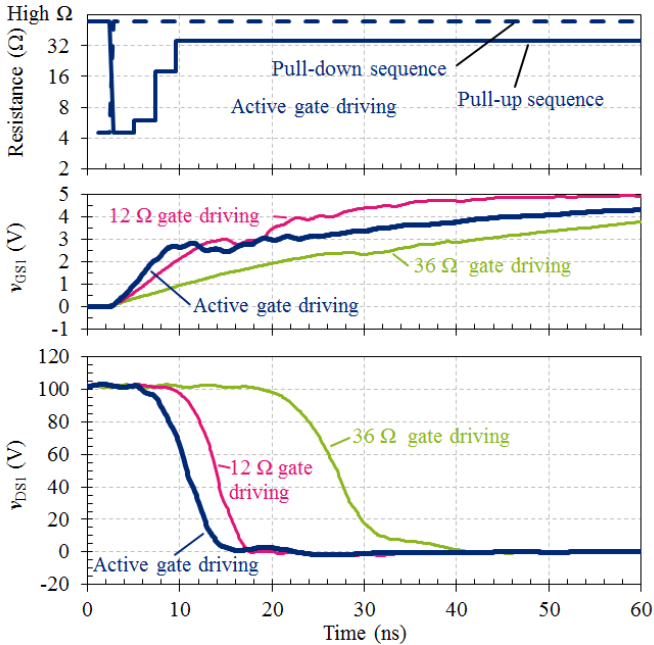


Fig. 10. Measured switch-node and low-side gate voltages, for fixed drive strengths of 12  $\Omega$  and 36  $\Omega$ , and for the active gate driving profile shown in the top graph. Profiling is seen to reduce switching delay.

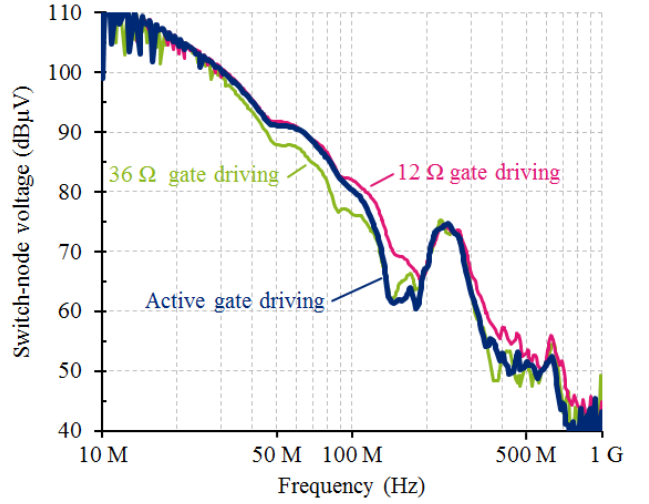


Fig. 11. Spectral envelopes, calculated from measured time-domain data, of the switch-node voltage waveform for the three gate-driving methods of Fig. 10. Active gate driving is seen to provide a drop in high-frequency content that is similar to an increase in gate resistance from 12 to 36  $\Omega$ .

scenarios. At frequencies above 125 MHz, the active gate drive results in switch-node high-frequency content matching that achieved with slow 36  $\Omega$  driving, that is up to 9 dB lower than the 12  $\Omega$  case. Therefore, spectral content is similar to, and in places better than, that given by using a large gate resistance value, without incurring higher switching loss associated with this higher gate resistance.

### V. CONCLUSIONS

This work has shown that active gate driving of 650 V GaN FETs is effective for a number of objectives. It has been possible to shape both the drain current and drain-source voltage of both power devices in a bridge leg in both buck- and boost-mode operation. The sub-nanosecond timing capability of the custom active gate driver is shown to be essential to allowing waveforms to be shaped. It was found that using a 0.2 nH/300 MHz current sensor facilitated the improvement of both current and voltage waveforms in the bridge-leg. The 150 ps resolution, and low driver impedance range (0.12 to 64  $\Omega$ ) permit the optimisation of mains-voltage GaN FET waveforms without the integration of the driver and device into a single package. In this work, the programmable gate driver is only using a small proportion of the available 319 output transistors, and therefore the 5 mm<sup>2</sup> silicon driver could be significantly reduced if targeted at this specific application. It is anticipated that the timing precision would need to be maintained.

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